REMARKS

The Examiner's Quayle Action of April 27, 2004 has been received and its contents reviewed. Applicants would like to thank the Examiner for indicating the allowance of claims 1-3.

In response to the Quayle Action, Applicants are submitting herewith a Request for Continuing Examination along with an Information Disclosure Statement and new claims 4-42. Accordingly, claims 1-42 are pending, of which claims 1, 13, 23 and 33 are independent.

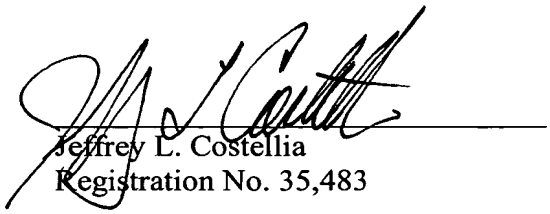
Turning now to the detailed Quayle Action, the specification stands objected to as containing various informalities. In response, Applicants have followed the Examiner's suggestions to overcome the informalities, which include providing a new title of the invention, cross reference to a related patent, and a new Abstract of the Disclosure.

Further, Applicants have amended claim 3 to correct a typographical error to change the dependency of original claim 3 from claim 14 to claim 1. Additionally, Applicants have added new claims 4-42 to further complete the scope to which Applicants are entitled.

Applicants respectfully note that the filing date of this instant application, which is shown as June 24, 2003 in all communications received from the U.S. Patent and Trademark Office thus far, is incorrect. This error on the Office's part has been brought to the attention of the Filing Receipt Corrections branch of the U.S. PTO via facsimile on January 8, 2004. Applicants respectfully request again that the filing date be corrected as June 26, 2003.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,



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ABSTRACT OF THE DISCLOSURE

A method of manufacturing a semiconductor with a storage capacitor having sufficient memory capacity while requiring a minimum area is provided. The method includes steps for manufacturing a storage capacitor of a pixel region that has a structure of a first storage capacitor and a second storage capacitor stacked on top of the other and connected in parallel with each other. The method further includes steps for forming the first storage capacitor having a first capacitance electrode formed in the same layer as a drain region, a first dielectric, and a second capacitance electrode formed in the same layer as a gate wiring. Still further, the method includes steps for forming the second storage capacitor including the second capacitance electrode, a second dielectric, and a third capacitance electrode formed in the same layer as a light-shielding film.